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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,534	02/06/2002	Ming Michael Li	97-P-149D1 (850063.518D1)	9996
30423	7590	10/04/2004		EXAMINER
STMICROELECTRONICS, INC.				ROCCHEGIANI, RENZO
MAIL STATION 2346				
1310 ELECTRONICS DRIVE			ART UNIT	PAPER NUMBER
CARROLLTON, TX 75006				2825

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/068,534	LI, MING MICHAEL	
	Examiner	Art Unit	
	Renzo N. Rocchegiani	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 06 February 2002.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-8 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

- Certified copies of the priority documents have been received.
- Certified copies of the priority documents have been received in Application No. _____.
- Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 02/06/2002.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: the reference to the parent application should be corrected to also state that the previous application is now US Patent No. 6,383,905 B2.

Appropriate correction is required.

2. Examiner also would like to notify applicant that the parent application that issued as US Patent No. 6,383,905 B2 has the name of the inventor misspelled.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,554,566 (Lur et al.).

Lur et al. discloses an integrated device comprising a semiconductor substrate (item 1), a polysilicon line (item 4) having a micro-rough indentations on the top surface (item 6B) and a silicide film (item 5) covering the top rough surface of the polysilicon

line. Lur et al. further disclose a plurality of isolation areas (items 2), a thin gate oxide (item 3) between the polysilicon line and the substrate and a plurality of patterned active regions on the substrate on the sides of the polysilicon line (Fig. 4). The polysilicon line forms a gate region (Fig. 4) with source and drain regions (items 7), the gate structure has sidewall spacers (items 8) and doped regions adjacent to the sidewall spacers (items 7). The silicide film comprises TiSi (col. 4, lines 35-45). Because the surface is rough the surface area is inherently larger. Finally a metallization structure is positioned on the silicide film to provide an interconnection. (items 11)

5. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 5,893,751 (Jenq et al.).

Jenq et al. discloses an integrated device comprising a semiconductor substrate (item 10), a polysilicon line (item 16) having a micro-rough indentations on the top surface (col. 2, lines 30-35) and a silicide film (item 27) covering the top rough surface of the polysilicon line. Jenq et al. further disclose a plurality of isolation areas (items 12), a thin gate oxide (item 14) between the polysilicon line and the substrate and a plurality of patterned active regions on the substrate on the sides of the polysilicon line (Fig. 2D). The polysilicon line forms a gate region (Fig. 2D) with source and drain regions (items 20), the gate structure has sidewall spacers (items 18) and doped regions adjacent to the sidewall spacers (items 20). The silicide film comprises TiSi (col. 3, lines 20-25). Because the surface is rough the surface area is inherently larger.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,554,566 (Lur et al.) in view of US Patent No. 5,654,589 (Huang et al.).

As stated in paragraph 4, all the limitations of this claim have been met except for teaching that the interconnection comprises a multilayer stack.

Huang et al. teaches forming an interconnection over a gate that has been capped with a silicide wherein the interconnection comprises a multilayer structure. (Fig. 1H).

It would have been obvious to one with ordinary skill in the specific art to combine the teachings of Huang et al. to those of Lur et al. and form a multilayer interconnection, since Huang et al. discloses that forming the interconnections with multiple layers as taught results in low sheet resistance and miniaturization as well as other benefits. (See Huang et al. col. 3, lines 35-67).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Renzo N. Rocchegiani whose telephone number is (571)272-1904. The examiner can normally be reached on Mon.-Fri. 8:00 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571)272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Renzo N. Rocchegiani
Examiner
Art Unit 2825



MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800